NEW UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. 1.53(b))

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Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

METHOD AND APPARATUS FOR REDUCING SUBSTRATE BIAS VOLTAGE DROP

and invented by:

Tongbi Jiang and Zhiqiang Wu

IF A CONTINUATION APPLICATION, check appropriate box and supply requisite information:

☐ Continuation ☐ Divisional

☐ Continuation-in-part (CIP) of prior application No.: _____

Enclosed are:

Application Elements

1. [X] Filing fee as calculated and transmitted as described below
2. [X] Specification having 39 pages(s) and including the following:
   - a. [X] Descriptive title of the invention
   - b. [ ] Cross references to related applications *(if applicable)*
   - c. [ ] Statement regarding Federally-sponsored research/development *(if applicable)*
   - d. [ ] Reference to microfiche appendix *(if applicable)*
   - e. [X] Background of the invention
   - f. [X] Brief summary of the invention
   - g. [X] Brief description of the drawings *(if drawings filed)*
   - h. [X] Detailed description
   - i. [X] Claims as classified below
   - j. [X] Abstract of the disclosure

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Application Elements (continued)

3. [X] Drawing(s) *(when necessary as prescribed by 35 U.S.C. 113)*

   [X] Formal [ ] Informal Number of sheets: 6

4. [X] Oath or Declaration

   a. [X] Newly executed (original or copy) [ ] Unexecuted

   b. [ ] Copy from a prior application (37 C.F.R. 1.63(d) *(for continuation/divisional applications only)*

   c. [ ] With Power of Attorney [ ] Without Power of Attorney

5. [ ] Incorporation by reference *(usable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. [ ] Computer program in microfiche

7. [ ] Genetic sequence submission *(if applicable, all must be included)*

   a. [ ] Paper copy

   b. [ ] Computer readable copy

   c. [ ] Statement verifying identical paper and computer readable copies

Accompanying Application

8. [X] Assignment papers *(cover sheet & document(s))*

9. [ ] 37 C.F.R. 3.73(b) statement *(when there is an assignee)*

10. [ ] English translation document *(if applicable)*

11. [ ] Information Disclosure Statement/PTO-1449 [ ] Copies of IDS citations

12. [ ] Preliminary Amendment

13. [X] Acknowledgment postcard

14. [ ] Certified copy of priority document(s) *(if foreign priority is claimed)*

15. [ ] Certificate of Mailing

    [ ] First Class [ ] Express Mail (Label No.: _____)

16. [ ] Small Entity statement(s) -- # submitted _____ *(if Small Entity status claimed)*

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Accompanying Application (continued)

17. ☐ Additional enclosures *(please identify below):*

Fee Calculation and Transmittal

The filing fee for this utility patent application is calculated and transmitted as follows:

☒ Large Entity ☐ Small Entity

CLAIMS AS FILED					
For	**# Filed**	**# Allowed**	**# Extra**	**Rate**	**Fee**
Total Claims	99	- 20 =	79	x $18.00	$1,422.00
Independent Claims	7	- 3 =	4	x $78.00	$312.00
Multiple Dependent Claims (check if applicable)			☐		
Other Fees (specify purpose):					
				BASIC FEE	$690.00
				TOTAL FILING FEE	$2,424.00

☒ A check in the amount of $2,424.00 to cover the total filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge and Deposit Account No. 4 - 1073 as described below. A duplicate copy of this sheet is enclosed.

☐ Charge the amount of _____ as filing fee.

☒ Credit any overpayment.

☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.

☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.31(b).

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
APPLICATION FOR U.S. LETTERS PATENT

Title:

METHOD AND APPARATUS FOR REDUCING SUBSTRATE BIAS VOLTAGE DROP

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BACKGROUND OF THE INVENTION

The invention relates to semiconductor devices and more particularly to a method and apparatus for reducing bias voltage drops within a substrate.

DESCRIPTION OF THE RELATED ART

Semiconductor devices which perform various functions are constructed on semiconductor substrates using a variety of techniques. The integrated circuits are generally constructed on the upper, active surface of a substrate or semiconductor wafer. It is common to provide a substrate bias voltage Vbb via a plurality of well plugs, such as P-well plugs. The Vbb bias voltage is typically provided by a voltage regulator or a charge pump. The well plugs are electrically connected with the substrate through respective diffusion regions. The substrate bias voltage Vbb is used to control the threshold voltage Vt of various transistors formed in the substrate and maintain a substantively uniform Vt from transistor to transistor. If the substrate voltage Vbb differs across the area of the

substrate due to voltage drops it changes the threshold voltage Vt characteristics of nearby transistors causing the transistors to switch inappropriately.

It is known in the art to maintain a stable substrate bias voltage Vbb over a large area of the substrate by spacing the well plugs close together, however this occupies large substrate real estate. It is also known to use a heavily doped substrates with a lightly doped epitaxial layer to help stabilize the substrate voltage; however such processes are expensive. It would be desirable to have a semiconductor device and method of making the same that cost effectively reduces bias voltage Vbb drop across the substrate, and which also reduces the number of P-well plugs required to supply the bias voltage Vbb over a given substrate area.

SUMMARY OF THE INVENTION

The invention provides a conductive layer secured to a backside of a semiconductor substrate to help maintain a more uniform level of bias voltage within the substrate. The substrate has transistors fabricated on its upper, active side and has P-well plugs on the

upper, active side that electrically couple Vbb voltage from a Vbb voltage source to the substrate. The conductive layer can be a conductive metallic layer, a conductive paste, a conductive polymeric film, or a conductive metallic film and provides a path for removing unwanted voltage or noise from the substrate to help maintain a uniform Vbb voltage throughout the substrate. As a consequence, a more uniform bias voltage Vbb is provided within the substrate and in particular in the proximity of the transistors and thus the number of P-well plugs used to supply the Vbb voltage can be reduced. The backside conductive layer may optionally be directly connected to a Vbb bias source.

Different materials and methods are disclosed for forming and/or securing the conductive layer to the backside of the substrate. In one exemplary embodiment the conductive layer is a metallic layer, which may optionally extend beyond the backside of the substrate to provide an area for a wire bond connection to the Vbb bias source. In other exemplary embodiments the conductive layer may be formed as a cureable conductive paste, a conductive polymeric film, or a thin conductive metal film.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other advantages and features of the invention will be more readily understood from the following detailed description of the invention which is provided in connection with the accompanying drawings.

FIG. 1 is a graphical representation of a change in transistor threshold voltage Vt caused by variations in substrate bias voltage Vbb.

FIG. 2 is a side view of an integrated circuit semiconductor device which is fabricated in accordance with the invention.

FIG. 3 is a block diagram of a semiconductor device voltage supply system with bias voltage Vbb connected to a P-well tie down and to a conductive layer used in the invention.

FIG. 4 is a top view of a semiconductor device with a conductive layer attached to the backside of the substrate in accordance with the invention.

FIG. 5 is a cross-sectional view of FIG. 4.

FIG. 6 is a schematic diagram of a typical processor system with which the invention may be used.

DESCRIPTION OF PREFERRED EMBODIMENTS

The invention will now be described with reference to a substrate of a semiconductor device which is biased by a Vbb voltage, which may be obtained from a pumped voltage source. It is understood that the invention has broader applicability and may be used with a substrate of any pumped or non-pumped semiconductor device, including processors and memory devices with many different circuit and transistor configurations. Similarly, the process and resulting structure described below are merely exemplary of the invention, as many modifications and substitutions can be made without departing from the spirit or scope of the invention.

The term "substrate" used in the following description may include any semiconductor-based structure that has an exposed silicon surface. Structure must be understood to include silicon, silicon-on insulator (SOI), silicon-on sapphire (SOS), doped and undoped semiconductors, epitaxial layers of silicon supported by a base

semiconductor foundation, and other semiconductor structures. The semiconductor need not be silicon-based. The semiconductor could be silicon-germanium, germanium, or gallium arsenide. When reference is made to substrate in the following description, previous process steps may have been utilized to form regions or junctions in or on the base semiconductor or foundation.

To help explain the invention a brief discussion of how the substrate bias voltage Vbb affects transistor operation is provided in connection with FIG. 1. It is a graphical representation 9 of the change in the threshold voltage Vt of a typical NMOS transistor fabricated in a substrate with variations in substrate bias voltage (Vbb). The x-axis is a measure of the bias voltage Vbb in volts and the y-axis measures the threshold voltage Vt of a transistor in volts. For FIG. 1 the transistor was designed to have a threshold voltage Vt of 0.65 Volts at a bias voltage Vbb of –1 volts. FIG. 1 demonstrates that as the bias voltage Vbb varies the transistor's threshold voltage Vt also varies. Accordingly, it is important to keep the Vbb bias voltage within a substrate as uniform as possible to avoid localized changes of transistor Vt which will affect transistor operation. However,

variations in bias voltage Vbb occur due to unwanted voltage or electrical noise that develops within and along a substrate. Some of this voltage comes from device "cross talk" while some of the unwanted voltage or electrical noise is generated from the operation of the various transistors themselves. While FIG. 1 illustrates the impact of substrate voltage drop on a transistor, it is understood that the present invention relates to semiconductor electrical elements in general, such as transistors, resistors, capacitors, electrodes, amplifiers, inverters, and gates.

Referring now to FIG. 2, is a partial elevation view of a semiconductor device 100 fabricated in accordance with the present invention. The present invention provides a conductive layer 60, such as a metallic layer, conductive paste, conductive polymeric film, or conductive metallic film, on the back side 81 of a semiconductor substrate 10 to maintain a more uniform bias voltage Vbb throughout substrate 10. The device 100 is shown with two exemplary MOSFET transistors 40, 42 constructed on substrate 10 which is formed of a semiconductor material with a P-well region 13, in the upper portion of substrate 10. Device 100 has top surface 91 and substrate upper surface 79 and backside

81. Conductive layer 60 is shown attached to the backside 81. Conductive layer 60 may be a metallic layer (first embodiment), a conductive paste (second embodiment), a conductive polymeric film (third embodiment), or a conductive metallic film (fourth embodiment). FIG. 2 shows conductive layer 60 formed as a metallic layer. Wire bond 95 is shown connecting conductive layer 60 with bonding pad 85. Bonding pad 85 may be in electrical contact with bias voltage Vbb source 92 and discussed with respect to FIGS. 3.

The FIG. 2 device 100 is merely exemplary of a typical solid state semiconductor circuit which could be configured in numerous ways. Various transistors 40, 42, P-well plug diffusion regions 14, field oxide regions 12, source/drain regions 16, and resistors 18 may be formed on the upper surface 79 of the substrate 10 or in P-well 13. The transistors 40, 42 are shown formed on gate oxide region 46, with a silicide layer 45, gate electrode 43, and a dielectric cap layer 44. The gate stacks 40, 42 are covered with a gate stack insulating layer or gate spacer 20 which may be silicon nitride. Gate insulation layer 20 and substrate 10 are also covered with insulating layer 11 which is typically

Borophosphosilicate glass (BPSG) or other suitable insulation material. Openings are formed in insulating layer 11 and electrically conductive plugs 30, 32, 34, and 36 are formed in the openings for contact with diffusion regions 14, 16, 17 of the substrate 10. P-well tie down plugs 30 are conventionally used to apply the bias voltage Vbb 92 to P-well 13 via P-well diffusion regions. Also shown are contact plugs 32 in contact with resistor 18 and contact plugs 34, 36 in contact with source/drain regions 16.

P-well plugs 30 are made of a conductive material with low resistance, such as tungsten or polysilicon, and serve as ohmic contact between the bias voltage Vbb source 92 shown in FIG. 3 and P-well 13. P-well plugs 30 may be connected to bias voltage Vbb 92 via metallization layer 90, bonding pads 83, and wire bonds 82 as shown in FIG. 4. The bias voltage Vbb 92 is transferred to P-well 13 from by P-well plugs 30 and P-well diffusion regions 14. Conductive layer 60 is shown wire bonded 95 to bonding pad 85.

In a first exemplary embodiment of the invention shown in FIG. 2 the conductive layer 60 is, as noted, preferably formed as a metallic layer. The metallic layer has a thickness preferably less than or equal to 10 mil. The conductive layer 60 may be secured

to the backside 81 of the substrate 10 by a conductive adhesive, such as "Ablebond 8360" manufactured by ABLESTIK Labs, Inc. The conductive layer 60 is preferably attached to the backside 81 after a fabricated wafer has been cut into individual semiconductor devices (dies) 100. The conductive layer 60 may extend beyond the length of the substrate 10, as shown at the left side of FIG. 2, to allow for attachment thereto of a bonding wire 95 which connects the conductive layer 60 to a bonding pad 85. The overall length of conductive layer 60 preferably extends no more than approximately 5 mils past substrate edge 8.

Conductive layer 60 should have a low resistivity preferably less than 1×10^{-8} Ohm-meter. Suitable metals, metal alloys, or compounds for conductive layer 60 may be selected from at least one of the following metals: copper (Cu), silver (Ag), alloy 42, gold (Au), iron (Fe), and aluminum (Al). Conductive layer 60 removes unwanted voltage or electrical noise from substrate 10 thus reducing undesirable localized drops in the substrate bias voltage Vbb. Conductive layer 60 can be directly connected to bias voltage Vbb 92 (FIG. 3), for example, the unwanted noise signal can move vertically downward

through substrate 10 to conductive layer 60 and flow through wire bond 95 to bonding pad 85. From bonding pad 85 it can flow to Vbb source 92 (FIG. 3) by known techniques.

Although FIG. 2 shows conductive layer 60 electrically connected to the bonding pad 85, benefits can also be achieved without directly connecting conductive layer 60 to bonding pad 85. In this case, conductive layer 60 attracts undesired voltages and or switching noise from localized regions of the substrate 10, such as P-well 13 and transfers it to other regions of substrate 10 thereby minimizing local Vbb voltage drops, such as at transistor gate stacks 40, 42.

In a second exemplary embodiment conductive layer 60 is formed of a curable conductive paste such as "Ablebond 8360". In this case conductive paste 60 may have the same length as the substrate 10. The conductive paste 60 may be a thermoplastic resin containing conductive particles. The conductive particles are preferably metal and may be selected from at least one of the following metals: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni) particles. The conductive paste 60 should have a

resistivity less than 1 x 10^{-5} Ohm-meter, preferably less than 1 x 10^{-7} Ohm-meter. The conductive paste 60 should have a thickness less than or equal to 1 mil, preferably less than approximately 0.5 mil. The cure time for the conductive paste 60 is preferably less than 15 minutes. The conductive paste 60 may be cured by heat and/or ultraviolet light. Conductive paste 60 can be applied to the substrate backside 81 of the wafer after backgrind but prior to cutting the wafer into individual semiconductor devices 100. Conductive paste 60 can be applied by spin coating, spraying, screen printing, or blade coating the paste 60.

Like the conductive metallic layer described above, if conductive paste 60 is not in direct electrical communication with bonding pad 85, it will still draw unwanted voltage or electrical noise away from substrate 10 to help stabilize the operation of the electrical elements of the device 100. Unwanted voltage noise in substrate 10 may exit the substrate 10 by moving vertically down substrate 10 to conductive paste 60 where it is flows through the conductive paste 60. For example, transferred noise in conductive paste 60 may horizontally flow away from gate stacks 40, 42 and re-enter substrate 10 in the

proximity of P-well diffusion regions 14. The noise can then flow from P-well diffusion regions 14 to P-well plugs 30. From the P-well plugs 30, the voltage can flow to bonding pads 83, via metalization layers 90, where it can further flow away from active areas of device 100.

In a third exemplary embodiment, conductive layer 60 is formed of a conductive polymeric film, such as "FC-262(b)" made by Hitachi Corporation. The conductive film 60 must be isotropically conductive, i.e., a three dimensional film, so that voltage is free to move in all three dimensions. A two dimensional film would not allow unwanted noise to move vertically through a two dimensional film. Conductive film 60 may be a solid resin matrix containing conductive particles. Conductive film 60 preferably has a thickness greater than approximately 1 mil and preferably less than approximately 3 mil. The conductive particles are preferably selected from at least one of the following metals: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni). Conductive film 60 should have a resistivity less than approximately 1×10^{-5} Ohm-meter, preferably less than 1×10^{-7} Ohm-meter. A conductive film 60 can be applied to the wafer backside 81 after

backgrind but prior to cutting the wafer into individual semiconductor devices 100. Conductive film 60 can be applied by applying pressure greater than approximately 1 MegaPascal (MPa) to the film and/or wafer, and preferably a pressure between approximately 1 to 5 (MPa) for preferably about 5 seconds or less. The conductive film 60 should be applied at a temperature greater than 175 degrees Celsius, and preferably a temperature range of approximately 175 to 400 degrees Celsius. Conductive film 60, like the conductive paste, will draw unwanted voltage or electrical noise away from substrate 10 in the manner described above with respect to the conductive paste.

In a fourth exemplary embodiment, conductive layer 60 is formed of a conductive metallic film 60. The conductive film 60 preferably should have a thickness less than or equal to approximately 1 mil and is preferably formed of conductive particles selected from the following metals: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni). Conductive film 60 should have a resistivity less than approximately 1×10^{-5} Ohm-meter, preferably less than 1×10^{-8} Ohm-Meter. Conductive film 60 can be applied to the substrate backside 81 after backgrind but prior to the cutting of the wafer into individual

semiconductor devices. The conductive film 60 can be applied by any of the following methods or techniques: electroless plating, electrolytic plating, molecular beam epitaxy (MBE), vapor phase epitaxy (VPE), physical vapor deposition (PVD), chemical vapor deposition (CVD) and metal organic chemical vapor deposition (MOCVD). Like the conductive paste, conductive metallic film 60 draws unwanted voltage or electrical noise away from substrate 10 in the same manner as described above with respect to the conductive paste.

FIG. 3 is a block diagram of a semiconductor device voltage supply system 200 which includes a substrate bias voltage Vbb source 92. Shown are an external voltage supply Vcc 97 which supplies voltage to Vbb source 92 via electrical contact 120. Vbb source 92 is shown supplied to P-well 13 through electrical contact 122, lead finger 87, wire bond 82, bonding pad 83, metalization layer 90, P-well contact plug 30, and P-well diffusion region 14. Conductive layer 60 is shown electrically connected to Vbb 92 via wire bond 95, bonding pad 85 and electrical contact 121.

Exemplary voltage values for bias voltage Vbb 92 are –1 volts and 0 volts. If conductive layer 60 is a metallic layer it is relatively easy to electrically connect it to Vbb source 92 in the manner shown and described with reference to FIGS. 2 and 3. If the conductive layer 60 is a conductive paste, conductive polymeric film, or conductive metallic film they may also be electrically connected to Vbb source 92 through a wire or other connection. However as noted earlier, the impact of noise is still reduced even if conductive layer 60 is not in direct electrical communication to Vbb source 92.

FIG. 4 is a top view of the FIG. 2 semiconductor device 100 fabricated in accordance with the invention. Lead fingers 87 are shown secured to the top side 91 of device 100. The device 100 has a conductive layer 60 secured to the back side of the device 100 and extending past the device perimeter 101. Bonding pads 83, 85 typically are provided over an exterior surface area of the completed device 100, such as top surface 91, and may be located on the perimeter or centered on the top surface 91 as shown in FIG. 4.

After fabrication is complete the semiconductor device 100 may be secured to a lead frame (not shown) via lead fingers 87 as shown in FIG. 4. Bonding pad 85 of device 100 is shown bonded to the conductive layer 60 by a wire bond 95. Bonding pad 85 can be configured to be in electrical communication with substrate bias voltage Vbb source 92. Thus one path for removing noise from substrate 10 is for the noise to travel through the substrate 10 to conductive layer 60 to bonding pad 85 via wire bond 95. The remaining bonding pads 83 which are not in contact with conductive layer 60 are shown connected to lead fingers 87 by wire bonds 82 in accordance with the electrical requirements of the circuit design. The wire bonding can be performed with various methods and materials known in the art. Even if bonding 85 is not directly connected to Vbb source 92, the negative impact of unwanted substrate voltage or noise can still be reduced.

FIG. 5 is a cross-sectional view of FIG. 4 taken at line V-V. Conductive layer 60 is shown attached to the substrate bottom surface 81 with a conductive adhesive 62. Lead fingers 87 are shown attached to the top surface 91 of device 100 by a conductive

adhesive compound 94 using well known lead on chip techniques. Also shown is bonding pad 85 which is in electrical communication with conductive layer 60 via wire bond 82.

FIG. 6 illustrates a typical processor based system 102, including a DRAM memory device 108 and at least one or both of the processor and memory devices are fabricated according to the invention as described above. A processor based system, such as a computer system 102, generally comprises a central processing unit (CPU) 112, for example a microprocessor, that communicates with one or more input/output devices 104, 106 over a bus 118. The computer system 102 also includes a read only memory device (ROM) 110 and may include peripheral devices such as floppy disk drive 114 and a CD ROM drive 116 which also communicates with the CPU 112 over the bus 118. At least one of the CPU 112, ROM 110 and DRAM 108 has a conductive layer 60 attached to the backside of its substrate as described above.

Having thus described in detail preferred embodiments of the present invention, it is to be understood that the invention defined by the appended claims is not to be limited by particular details set forth in the above description as many apparent variations thereof

are possible without departing from the spirit or scope of the invention. Accordingly, the above description and accompanying drawings are only illustrative of preferred embodiments which can achieve the features and advantages of the present invention. It is not intended that the invention be limited to the embodiments shown and described in detail herein. The invention is only limited by the scope of the following claims.

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element circuit fabricated on an upper side of said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to said substrate; and

a conductive layer provided on a back side of said substrate.

2. The semiconductor device of claim 1, wherein said electrical element comprises at least one electrical element selected from the group consisting of transistors, resistors, capacitors, electrodes, amplifiers, inverters, and gates.

3. The semiconductor device of claim 1, wherein said conductive layer is electrically coupled to a terminal supplying said bias voltage.

4. The semiconductor device of claim 1 further comprising a plurality of conductive plugs for respectively coupling said bias voltage source to said distribution regions.

5. The semiconductor device of claim 1, wherein said conductive layer comprises a conductive metallic layer.

6. The semiconductor device of claim 5, wherein said conductive metallic layer has a thickness of less than or equal to 10 mil.

7. The semiconductor device of claim 5, wherein said conductive metallic layer is secured to the backside of said substrate with a conductive adhesive.

8. The semiconductor device of claim 5, wherein said conductive metallic layer is electrically coupled to a terminal supplying said bias voltage.

9. The semiconductor device of claim 5, wherein said conductive metallic layer has a resisitivity less than 1×10^{-8} Ohm-meter.

10. The semiconductor device of claim 5, wherein said conductive metallic layer comprises at least one material selected from the group consisting of copper (Cu), silver (Ag), alloy 42, gold (Au), iron (Fe), and aluminum (Al).

11. The semiconductor device of claim 10, wherein said conductive metallic layer is formed of at least one material selected from the group consisting of: copper (Cu), silver (Ag), alloy 42, gold (Au), iron (Fe), and aluminum (Al).

12. The semiconductor device of claim 5, wherein said metallic layer has at least one length which exceeds a length of said substrate.

13. The semiconductor device of claim 1, wherein said conductive layer comprises a cured conductive paste.

14. The semiconductor device of claim 13, wherein said conductive paste has a thickness of less than or equal to 1 mil.

15. The semiconductor device of claim 13, wherein said conductive paste has a resistivity less than 1×10^{-5} Ohm-meter.

16. The semiconductor device of claim 13, wherein said conductive paste comprises a material with conductive particles therein.

17. The semiconductor device of claim 16, wherein said conductive particles comprise at least one of the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

18. The semiconductor device of claim 1, wherein said conductive layer comprises an isotropically conductive polymeric film.

19. The semiconductor device of claim 18, wherein said conductive polymeric film has a thickness greater than 1 mil.

20. The semiconductor device of claim 18, wherein said conductive polymeric film has a resistivity less than 1×10^{-5} Ohm-meter.

21. The semiconductor device of claim 18, wherein said conductive polymeric film comprises at least one conductive particle selected from the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

22. The semiconductor device of claim 1, wherein said conductive layer comprises a conductive metallic film.

23. The semiconductor device of claim 22, wherein said conductive metallic film has a thickness of less than or equal to 1 mil.

24. The semiconductor device of claim 22, wherein said conductive metallic film has a resistivity less than 1 x 10^{-5} Ohm-meter.

25. The semiconductor device of claim 22, wherein said conductive metallic film comprises at least one material selected from the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

26. The semiconductor device of claim 25, wherein said conductive metallic film is formed of at least one material selected from the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

27. The semiconductor device of claim 1, wherein said device is a memory device.

28. The semiconductor device of claim 27, wherein said memory device is a dynamic random access memory (DRAM) device.

29. The semiconductor device of claim 1, wherein said device is a logic device.

30. The semiconductor device of claim 1, wherein said device is a processor device.

31. A method of forming a semiconductor device, said method comprising:

fabricating at least one electrical element on an upper side of a semiconductor substrate;

fabricating a plurality of bias voltage distribution regions over said upper side of said substrate for receiving a bias voltage and applying said bias voltage to said substrate; and

securing a conductive layer to a backside of said substrate.

32. The method of claim 31, wherein said electrical element comprises at least one electrical element selected from the group consisting of transistors, resistors, capacitors, electrodes, amplifiers, inverters, and gates.

33. The method of claim 31, wherein said conductive layer comprises a conductive metallic layer.

34. The method of claim 33, said conductive metallic layer has a thickness of less than or equal to 10 mil.

35. The method of claim 33, wherein said conductive metallic layer is secured to said substrate backside with a conductive adhesive.

36. The method of claim 33, further comprising coupling said conductive metallic layer to a terminal for supplying said bias voltage.

37. The method of claim 33, wherein said conductive metallic layer has a resisitivity less than between 1 x 10^{-8} Ohm-meter.

38. The method of claim 33, wherein said conductive metallic layer comprises at least one material selected from the group consisting of: copper (Cu), silver (Ag), alloy 42, gold (Au), iron (Fe), and aluminum (Al)

39. The method of claim 38, wherein said conductive metallic layer is formed of as least one material selected from the group consisting of: copper (Cu), silver (Ag), alloy 42, gold (Au), iron (Fe), and aluminum (Al).

40. The method of claim 33, wherein said conductive metallic layer has at least one length which exceeds a length of said substrate.

41. The method of claim 33, wherein said conductive metallic layer is applied to said substrate back side after a fabricated wafer is cut into individual semiconductor devices.

42. The method of claim 31, further comprises providing a plurality of conductive plugs for respectively coupling a received bias voltage source to said distribution regions.

43. The method of claim 31, wherein said conductive layer comprises a cured conductive paste.

44. The method of claim 43, wherein said conductive paste has a thickness less than or equal to 1 mil.

45. The method of claim 43, wherein said conductive paste has a resistivity less than 1 x 10^{-5} Ohm-meter.

46. The method of claim 43, wherein said conductive paste is formed of a material comprising conductive particles.

47. The method of claim 43, wherein said conductive paste comprises conductive particles selected from at least one of the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

48. The method of claim 43, further comprising applying said conductive paste to the backside of a fabricated wafer after the wafer is background and before the wafer is cut into individual semiconductor devices.

49. The method of claim 31, wherein said conductive layer comprises an isotropically conductive polymeric film.

50. The method of claim 49, wherein said conductive polymeric film has a thickness greater than about 1 mil.

51. The method of claim 49, wherein said conductive polymeric film has a resistivity less than 1×10^{-5} Ohm-meter.

52. The method of claim 49, wherein said conductive polymeric film comprises conductive particles selected from at least one of the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

53. The method of claim 49, further comprising applying said conductive polymeric film to the backside of a fabricated wafer after said wafer is background and before said wafer is cut into individual semiconductor devices.

54. The method of claim 49, wherein said conductive polymeric film is applied at a temperature greater than about 175 degrees Celsius.

55. The method of claim 49, wherein said conductive polymeric film is pressed against said substrate at a pressure greater than 1 mega Pascal.

56. The method of claim 31, wherein said conductive layer comprises a conductive metallic film.

57. The method of claim 56, wherein said conductive metallic film has a thickness of less than or equal to 1 mil.

58. The method of claim 56, wherein said conductive metallic film has a resistivity less than 1 x 10^{-5} Ohm-meter.

59. The method of claim 56, wherein said conductive metallic film comprises conductive particles selected from at least one the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

60. The method of claim 56, further comprising applying said conductive metallic film to the backside of a fabricated wafer after said wafer is background and before said wafer is cut into individual semiconductor devices.

61. The method of claim 56, wherein said conductive metallic film is deposited by a method selected from the group consisting of: electroless plating, electrolytic plating, molecular beam epitaxy (MBE), vapor phase epitaxy (VPE), physical vapor deposition (PVD), chemical vapor deposition (CVD) and metal organic chemical vapor deposition (MOCVD).

62. The method of claim 31, wherein said device is a memory device.

63. The method of claim 62, wherein said memory device is a dynamic random access memory (DRAM) device.

64. The method of claim 31, wherein said device is a logic device.

65. The method of claim 31, wherein said device is a processor device.

66. A processor system comprising:

a processor;

a memory device in electrical communication with said processor;

at least one of said memory device and said processor comprising:

a semiconductor substrate;

at least one electrical element fabricated on an upper side of said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to said substrate; and

a conductive layer provided on a back side of said substrate.

67. The system of claim 66, wherein said electrical element comprises at least one electrical element selected from the group consisting of: transistors, resistors, capacitors, electrodes, amplifiers, inverters, and gates.

68. The system of claim 66, wherein said conductive layer is electrically coupled to a terminal supplying said bias voltage.

69. The system of claim 66, further comprising plurality of conductive plugs for respectively coupling said bias voltage to said distribution regions.

70. The system of claim 66, wherein said conductive layer comprises a conductive metallic layer.

71. The system of claim 70, wherein said conductive metallic layer has a thickness of less than or equal to 10 mil.

72. The system of claim 70, wherein said conductive metallic layer is secured to the backside of said substrate with a conductive adhesive.

73. The system of claim 70, wherein said conductive metallic layer is electrically coupled to a terminal for supplying said bias voltage.

74. The system of claim 70, wherein said conductive metallic layer has a resisitivity less than 1×10^{-8} Ohm-meter.

75. The system of claim 70, wherein said conductive metallic layer comprises at least one material selected from the group consisting of: copper (Cu), silver (Ag), alloy 42, gold (Au), iron (Fe), and aluminum (Al).

76. The system of claim 75, wherein said conductive metallic layer is formed of at least one material selected from the group consisting of: copper (Cu), silver (Ag), alloy 42, gold (Au), iron (Fe), and aluminum (Al).

77. The system of claim 70, wherein said conductive metallic layer has a length which exceeds a length of said substrate.

78. The system of claim 66, wherein said conductive layer comprises a cured conductive paste.

79. The system of claim 78, wherein said conductive paste has a thickness of less than or equal to 1 mil.

80. The system of claim 78, wherein said conductive paste has a resistivity less than 1 x 10^{-5} Ohm-meter.

81. The system of claim 78, wherein said conductive paste comprises a resin with conductive particles.

82. The system of claim 81, wherein said conductive paste comprises at least one conductive particle selected from the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

83. The system of claim 66, wherein said conductive layer comprises an isotropically conductive polymeric film.

84. The system of claim 83, wherein said conductive polymeric film has a thickness greater than 1 mil.

85. The system of claim 83, wherein said conductive polymeric film has a resistivity less than 1×10^{-5} Ohm-meter.

86. The system of claim 83, wherein said conductive polymeric film comprises at least one conductive particle selected from the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

87. The system of claim 66, wherein said conductive layer comprises a conductive metallic film.

88. The system of claim 87, wherein said conductive metallic film has a thickness of less than or equal to 1 mil.

89. The system of claim 87, wherein said conductive metallic film has a resistivity less than 1×10^{-5} Ohm-meter.

90. The system of claim 87, wherein said conductive metallic film comprises at least one material selected from the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

91. The system of claim 90, wherein said conductive metallic film is formed of at least one material selected from the group consisting of: copper (Cu), silver (Ag), gold (Au), iron (Fe), and nickel (Ni).

92. The system of claim 66, wherein said device is a memory device.

93. The system of claim 92, wherein said device is a dynamic random access memory (DRAM) device.

94. The system of claim 66, wherein said device is a logic device.

95. The system of claim 66, wherein said device is a processor device.

96. A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element fabricated on said substrate; and

a conductive layer provided on a backside of said substrate, said conductive layer forming an electrical path between said substrate and at least one non-substrate area of said device.

97. A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element fabricated on an upper side of said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to at least some portion of said substrate; and

a conductive layer provided on a backside of said substrate, said conductive layer forming an electrical path between said substrate and said bias voltage source.

98. A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element fabricated on said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to at least some portion of said substrate;

a conductive metallic layer provided on a backside of said substrate, said conductive metallic layer wire bonded to a bonding pad of said semiconductor device; and

said bonding pad forming an electrical path between said conductive metallic layer and at least one other area of said device.

99. A semiconductor device comprising:

a semiconductor substrate;

at least one electrical element fabricated on said substrate;

a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to at least some portion of said substrate; and

a conductive layer provided on a backside of said substrate, said conductive layer in electrical communication with a bonding pad of said semiconductor device.

ABSTRACT

A semiconductor device is provided with a conductive layer provided on a backside of a semiconductor substrate. The conductive layer helps maintain a uniform bias voltage over the substrate. The conductive layer can also be used to apply a bias voltage to the substrate and reduce the number of bias voltage distribution regions required.

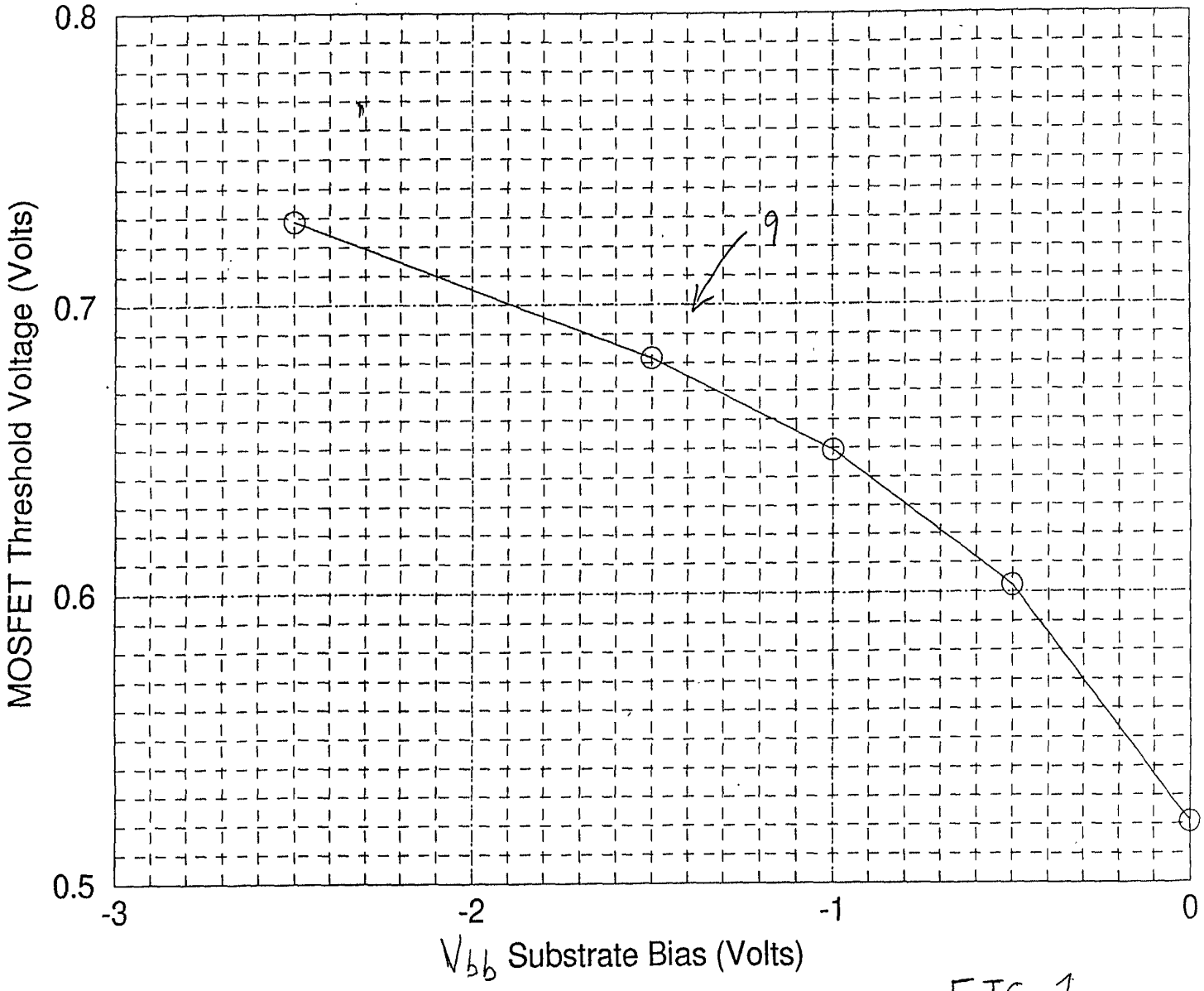
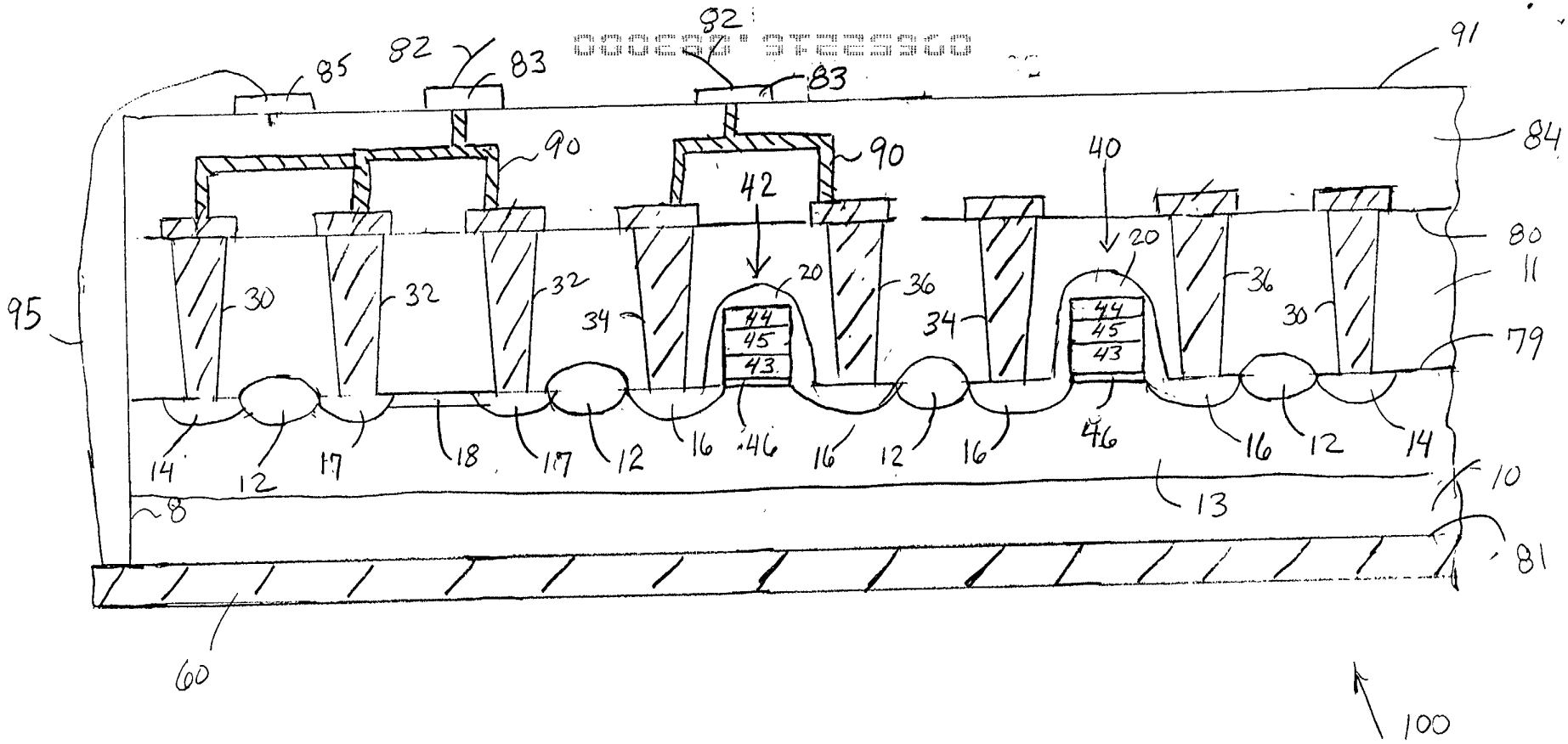

0.8
0.7
0.6
0.5
MOSFET Threshold Voltage (Volts)
-3
-2
-1
0
V_{bb} Substrate Bias (Volts)
9

FIG. 1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43
79
14
12
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10
13
8
81
60
100

FIG. 2

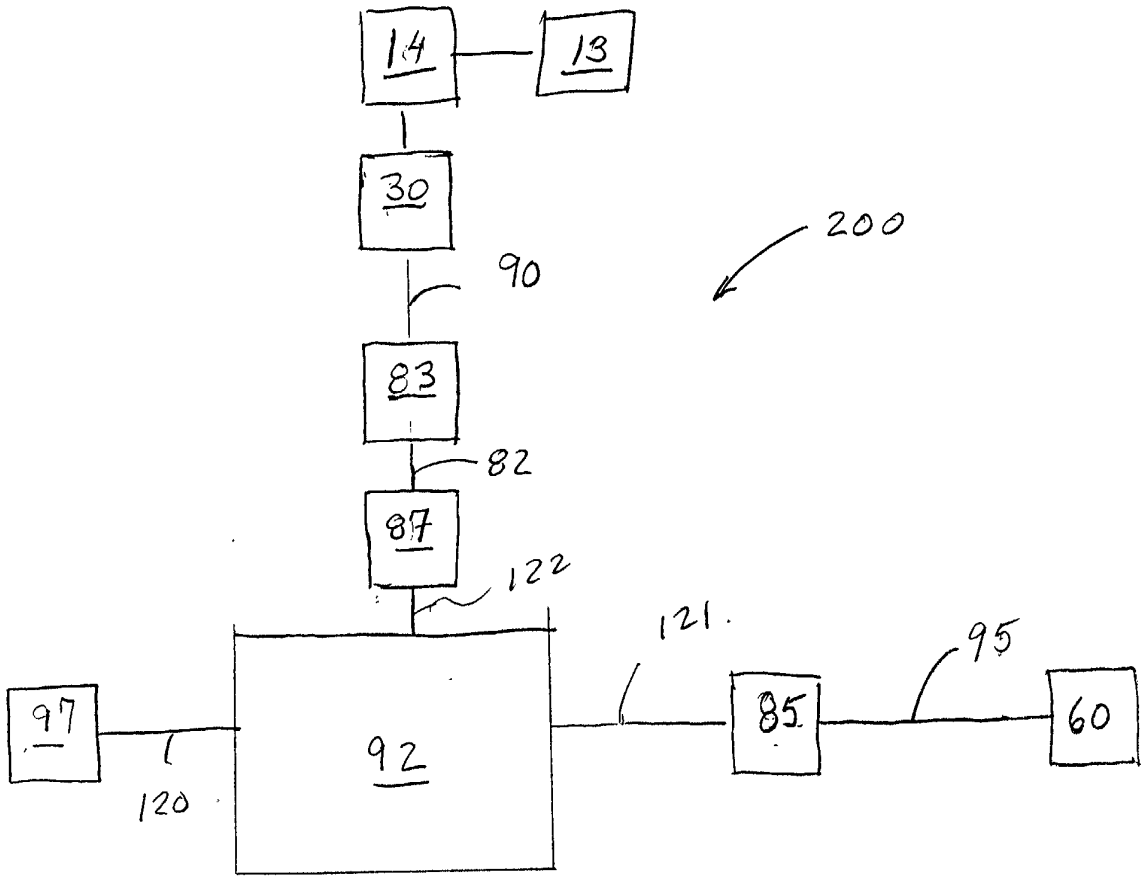

FIG. 3

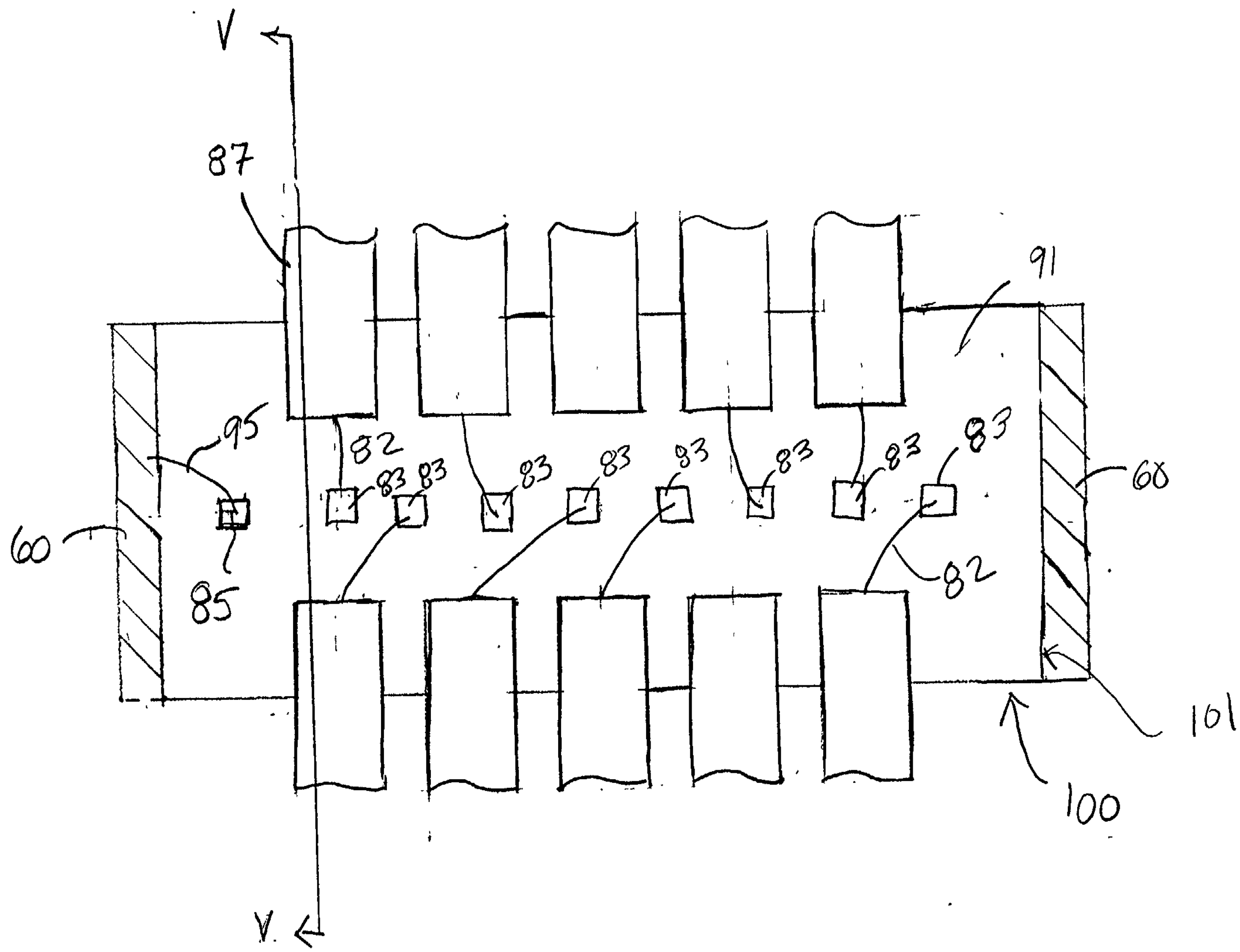

FIG. 4

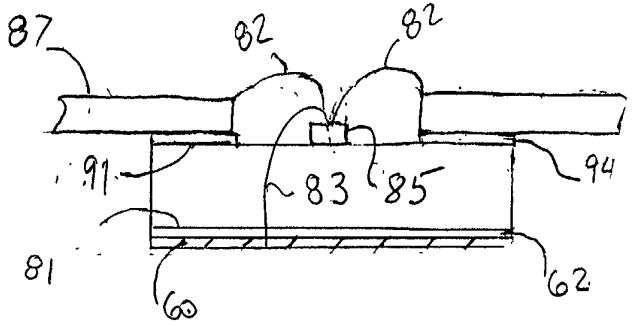

FIG 5

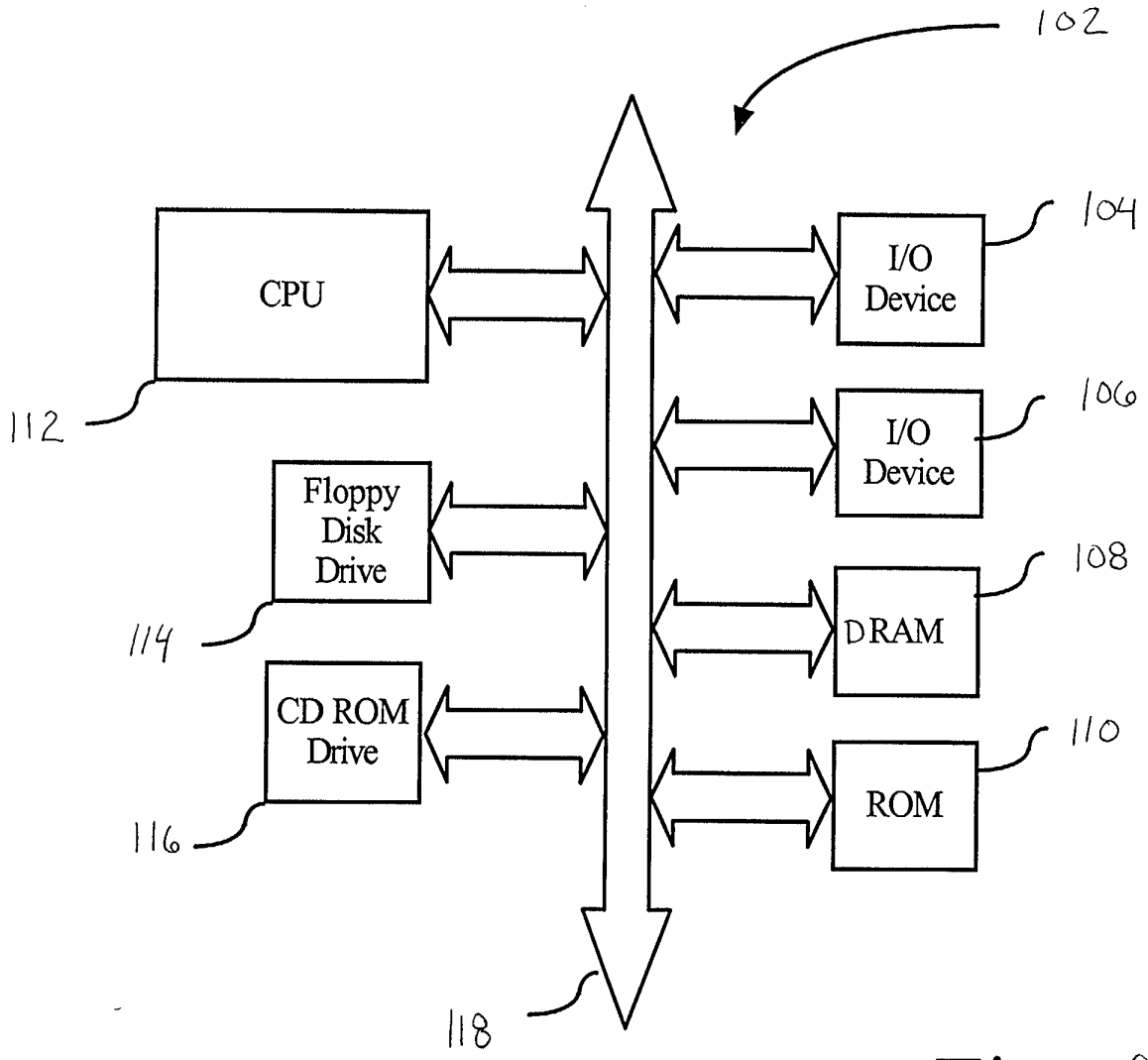
102
CPU
112
Floppy Disk Drive
114
CD ROM Drive
116
118
I/O Device
104
I/O Device
106
DRAM
108
ROM
110

Fig. 6

Docket No.: M4065.0227/P227
Micron No.: 96-1123

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD AND APPARATUS FOR REDUCING SUBSTRATE BIAS VOLTAGE DROP

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to in this oath or declaration.

I acknowledge the duty to disclose all information known to me which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code §119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

NONE

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

NONE

Docket No.: M4065.0227/P227
Micron No.: 96-1123

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Please address all correspondence to Thomas J. D'Amico of Dickstein Shapiro Morin & Oshinsky LLP located at 2101 L Street NW

Washington, DC 20037-1526. Telephone calls should be made to (202) 785-9700.

Full name of first inventor: Tongbi Jiang

Inventor's signature: _____ Date: 8-29-00

Residence: Boise, Idaho

Citizenship: United States of America

Post Office Address: 12036 W. Patrina Drive
Boise, ID 83713

Docket No.: M4065.0227/P227
Micron No.: 96-1123

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

DECLARATION FOR PATENT APPLICATION

Signature Page for Second Inventor

Full name of second inventor: Zhiqiang Wu

Inventor's signature: _____ Date: _____

Residence: Plano, Texas

Citizenship: United States of America

Post Office Address: 4012 Mildenhall Drive
Plano, Texas 75093

Docket No.: M4065.0227/P227
Micron No.: 96-1123

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

METHOD AND APPARATUS FOR REDUCING SUBSTRATE BIAS VOLTAGE DROP

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to in this oath or declaration.

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I hereby claim foreign priority benefits under Title 35, United States Code §119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

NONE

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

NONE

Docket No.: M4065.0227/P227
Micron No.: 96-1125

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Please address all correspondence to Thomas J. D'Amico of Dickstein Shapiro Morin & Oshinsky LLP located at 2101 L Street NW

Washington, DC 20037-1526. Telephone calls should be made to (202) 785-9700.

Full name of first inventor: Tongbi Jiang

Inventor's signature: _____ Date: _____

Residence: Boise, Idaho

Citizenship: China

Post Office Address: 12036 W. Patrina Drive
Boise, ID 83713

Docket No.: M4065.0227/P227
Micron No.: 96-1128

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

DECLARATION FOR PATENT APPLICATION

Signature Page for Second Inventor

Full name of second inventor: Zhiqiang Wu

Inventor's signature: _____ Date: 08/28/00

Residence: Plano, Texas

Citizenship: United States of America

Post Office Address: 4012 Mildenhall Drive
Plano, Texas 75093